CS6510

Product Brief JPEG2000 Encoder

The CS6510 JPEG2000 Encoder is a high performance application specific solution enabling leading edge image compression and transmission applications. The core is fully compliant with the ISO/IEC 15444-1 JPEG2000 Image Coding System Standard and makes possible both lossless and lossy compression of image data at ratios of up to 50:1. The CS6510 is capable of sustaining data rates of 3 cycles per sample enabling the compression of full motion, full colour video images. Equally suited to low-power, battery-operated consumer electronics as it is to high-end professional video equipment, the CS6510delivers the optimum image compression performance that only an application specific accelerator core canprovide. The CS6510 is a powerful and flexible JPEG 2000 encoding solution.

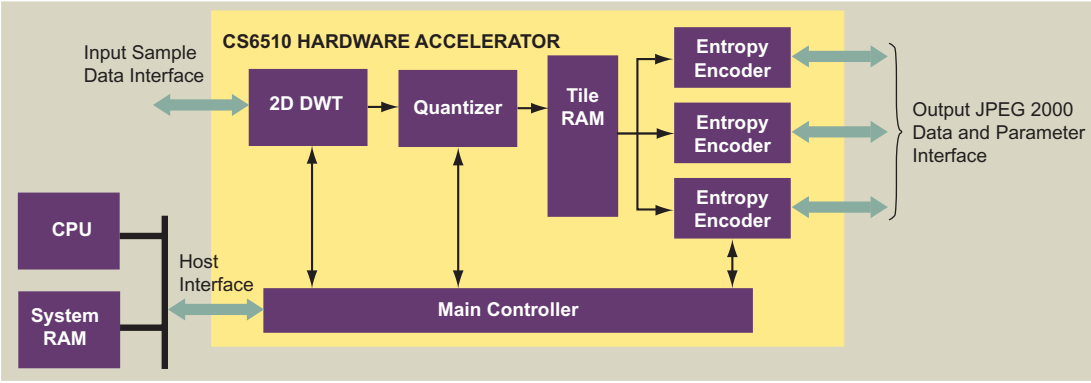

Figure 1: Amphion CS6510 JPEG2000 Encoder Hardware Accelerator

KEY FEATURES

- **Fully compliant with ISO/IEC 15444-1 JPEG 2000 Image Coding Standard: Part1 Profile 0**
- **Includes both 9/7 and 5/3 forward wavelet transforms with optimized line based memory utilization**
- **Very high data encoding rates**
- **Hardware accelerated rate control**
- **Flexible Input Image Format with up to 12 bits per image data sample**
- **Fully synchronous, single clocked cycle design**

KEY METRICS[1]

- **Logic:** 172k gates
- **Memory:** 50.5 KB
- **Performance:** 3 cycles per sample

APPLICATIONS

- **Megapixel Digital Still cameras**
- **Wireless PDA**
- **3G and 4G mobile telephone imaging applications**
- **SVGA-quality PC webcams**
- **Digital CCTV for remote/security surveillance**
- **Video-conferencing systems**
- **Video and imaging distribution systems: both wireless and networked**
- **Broadcasting stations up to SDTV rates**
- **Digital Cinema**
- **Hard disk drive Digital Video Recording and Editing**
- **Satellite imaging applications**

1. Performance is dependent on the silicon process and libraries selected.

FUNCTIONAL DESCRIPTION

The Amphion JPEG2000 encoder is an optimized, high performance hardware core which is fully compliant with the ISO/IEC 15444-1 JPEG2000 standard. Designed for the maximum levels of data throughput, the Amphion JPEG2000 solution addresses a wide variety of still and motion imaging applications up to the challenging limits of frame-based video compression for digital cinema applications and beyond. The flexible solution can be tailored to compress a variety of grayscale and color imaging formats producing superior low-bit rate performance down to 0.25bpp for highly detailed grayscale images. The solution also includes a variety of customizable functionality to allow the reconstruction of images with different resolutions and pixel accuracy for efficient display and delivery.

The Amphion JPEG2000 encoder has been developed to interface directly with the main system processor to provide a practical and complete JPEG2000 solution. All interfaces are AMBA compliant to facilitate integration into larger SOC systems. The encoding of an image is achieved via a two stage operation. The first stage of coding for each tile (Tier-1) is accomplished with a dedicated hardware accelerator, the CS6510. This accelerator is supplied with AHB bus DMA controllers for reading data to and from the core. On completion of Tier 1 coding the output bitstream (JP2 file) is created by Tier 2 software running on the host processor.

To compress an image, the source data, in any color space format, is read tile-by-tile into the CS6510 core. The forward discrete wavelet transform analyses the input data and passes it on to the quantizer where the first phase of data compression is enabled. When sufficient data has been quantized it is read, one codeblock at a time, and is passed to one of a number of entropy encoders. The entropy coding efficiently compresses the image data and the encoded bitstream is output in parallel with distortion metrics for the compressed data. These distortion metrics are examined by the Tier-2 software running on the main system CPU and are used to organize and truncate the compressed image data to facilitate rate control. The software then re-orders the bitstream into a user defined order, such as SNR progressive, based upon the rate-distortion information. To complete the encoding, the software builds the file header and file marker information and places this in the code stream along with the selected entropy coded data. The output is a complete JPEG2000 bitstream.

Figure 2 outlines the in-system operation of the Amphion JPEG2000 Encoder.

DISCRETE WAVELET TRANSFORM

The Amphion JPEG2000 encoder contains compact high performance implementations of both the real irreversible 9-7 wavelet transform and the integer reversible 5-3 integer wavelet transform. The user can specify which wavelet is required via the host interface. The inclusion of both these wavelet types facilitates lossy and lossless compression which is fully compliant with the JPEG2000 standard. The CS6510 core can also be programmed with a configurable level of wavelet decompositions levels, up to a maximum of 5 levels. This facilitates high levels of granularity in the compressed JPEG2000 stream and allows for the reconstruction of images with different resolutions for efficient display and delivery. This high number of wavelet decomposition levels also enables a variety of different sized thumbnail images to be produced.

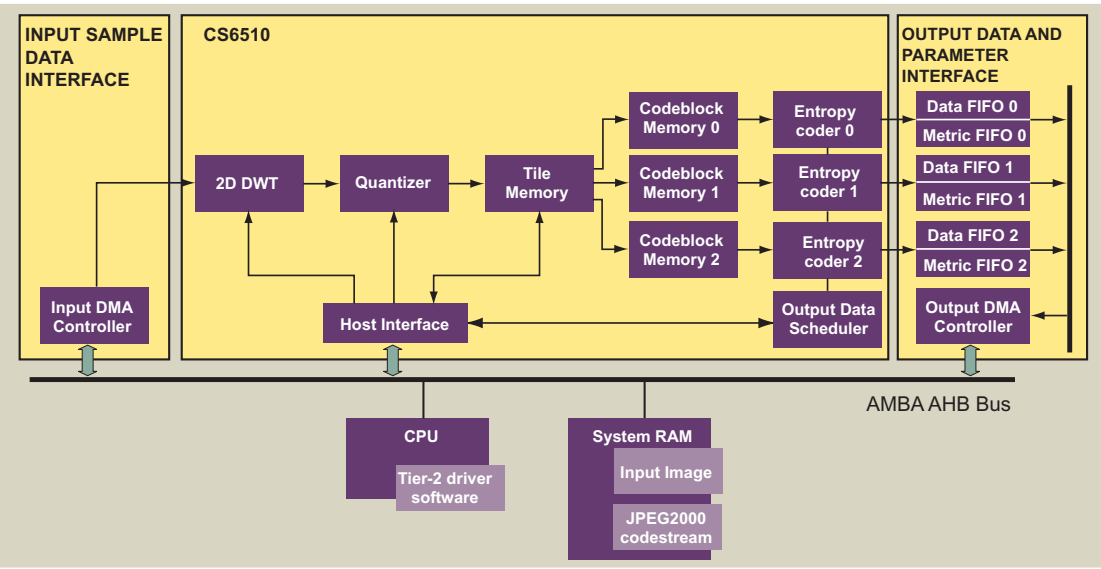

Figure 2: JPEG2000 Encoder Functional Block Diagram

The architecture employed for both the 9-7 and 5-3 wavelets is row-based. The optimized design minimizes the internal memory requirements of the core whilst maintaining the highest levels of data throughput (one sample/clock cycle processing for full-sized tile dimensions). The core accepts input data up to 12 bits, presented in raster order within the tile. The wavelet transform has also been developed to a high level of computational accuracy and exhibits a peak signal to noise ratio (PSNR) of greater than 60dB for up to and including five levels of wavelet decomposition.

COEFFICIENT QUANTIZER

Following wavelet transformation, the wavelet coefficients are quantized using a scalar quantization with deadzone technique. Distinct quantization values are employed for the coefficients of each sub-band; these are programmable by the user, depending on the required level of data compression. A maximum of 16 discrete quantization values are allowed for each tile (suffice for up to 5 levels of wavelet decomposition). For multi-component systems the quantization values are reprogrammed on a per-component basis. The coefficient quantizer quantizes one sample per clock cycle. For lossless compression using the 5/3 integer wavelet quantizer step sizes are always fixed at one effectively bypassing the quantization.

ENTROPY ENCODER

Within the JPEG2000 system the entropy encoders compress the source data and manipulate it such that it is suitable for the formation of layers and for progressive output. This enables tremendous flexibility in the output bitstream formation. To maintain the continuous high levels of data throughput the Amphion JPEG2000 encoder contains three entropy encoder blocks operating in parallel. Following quantization, each sub-band of the transformed tile is divided into rectangular code-blocks (32x32 or one complete codeblock per subband). Each codeblock is then coded independently in one of the three entropy encoders in a round-robin scheduling scheme. The first stage of the encoding is the segmentation of the image codeblock into horizontal bitplanes. These individual bitplanes are then coded using a 3 pass scanning system. The first plane to be coded is that which contains a non-zero magnitude bit. Processing then proceeds from the most significant to the least significant bit plane for the block. Following entropy encoding, the CS6510 core outputs 32-bit compressed image data in parallel with distortion metrics which describe the compressed data. These distortion metrics are examined by the Tier-2 software running on the main system CPU and are used to organize and truncate the compressed image data to facilitate rate control.

TIER-2 ENCODING SOFTWARE

To complete the JPEG2000 encode operation, Tier-2 control software is required to operate along with the CS6510 hardware component. This control software iterates through the component data on a tile-per-tile basis, and forms the output compressed JPEG2000 bitstream (JP2 file). The first stage of the Tier-2 coding operation involves reading the compressed image data and rate-distortion information from the CS6510 hardware core, via the DMA output interface. The rate-distortion data describes the contribution that each individual coding pass makes to the overall compressed image size. The software then calculates the distortion reduction associated with each coding pass and elects whether to include it in the final bitstream or not, based on the user defined target compression ratio. Both the compressed tile data and distortion metrics are stored in the system memory until all the constituent code-blocks in the image tile have been coded. The software then re-orders and truncates the bitstream into the chosen order (e.g. component, resolution-level progressive) based upon the rate-distortion information. The software also build up the file header information and place this in the code stream along with the selected entropy coded data. This control software is supplied for the Amphion JPEG2000 solution as standard C source code and can be easily ported to the target processor platform as required.

INPUT AND OUTPUT INTERFACES

The input and output data interfaces for the JPEG2000 encoder system are typically AMBA AHB (Advanced High-Speed bus) master compliant DMA modules and are supplied by Amphion in verilog source format. These deliverables act as example application specific implementations for writing and reading the input and output data sets from the CS6510 core to the system memory. As such the modules can be directly configured to the required parameters of the users system. The input interface DMA reads image data from the image memory and provides it to CS6510 core on a tile-by-tile basis. It is assumed that image data will be available in a linear memory in a raster scan order. The input interface is AMBA bus compatible with the image memory acting as an AMBA slave and the read input from the input DMA controller acting as an AMBA Master on the AMBA AHB. The output interface DMA reads the compressed tile data and distortion metrics directly from the individual entropy coders and stores the data in FIFO-style buffers. The output DMA then schedules the writing of the data to three distinct system memory locations, one for each entropy encoder. An AMBA AHB slave interface facilitates the programming of registers to define the required memory locations.

AVAILABILITY AND IMPLEMENTATION INFORMATION

DELIVERABLES

- Targeted optimized netlist for chosen technology (SoC or FPGA)
- Bit-accurate C-model
- Simulation model for system integration
- Source level software for Tier2 encoding and data stream formation
- Verilog source code for DMA input and output controllers
- Test Suite (standalone self-checking test-bench which incorporates control software via PLI with reference test data)
- Synthesis scripts
- Documentation (Integration, Simulation, Application and Function databooks)
- Technical support

ABOUT AMPHION

Amphion is the leading supplier of silicon-proven semiconductor intellectual-property (IP) for digital video and imaging System-on-a-Chip (SoC), ASIC and programmable logic (FPGA) designs, delivering high performance solutions for video and image compression with a comprehensive range of silicon-optimized products. Amphion develops and licenses semiconductor IP cores that are close to optimal in terms of power, cycles, and area. Amphion cores operate standalone, or by in conjunction with industry-standard RISC processors, and can be easily migrated through successive generations of fabrication technology.

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