Product Brief

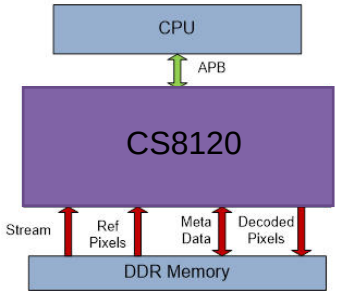
CS8120 HEVC/H.265 4Kp60 Video Decoder IP

Production Proven – HEVC/H.265 4Kp60 – Video Decoder

- Mature video decoder
- Silicon proven in multiple STB and DTV chipsets
- Hardware decoder paired with a RISC controller to perform video decode

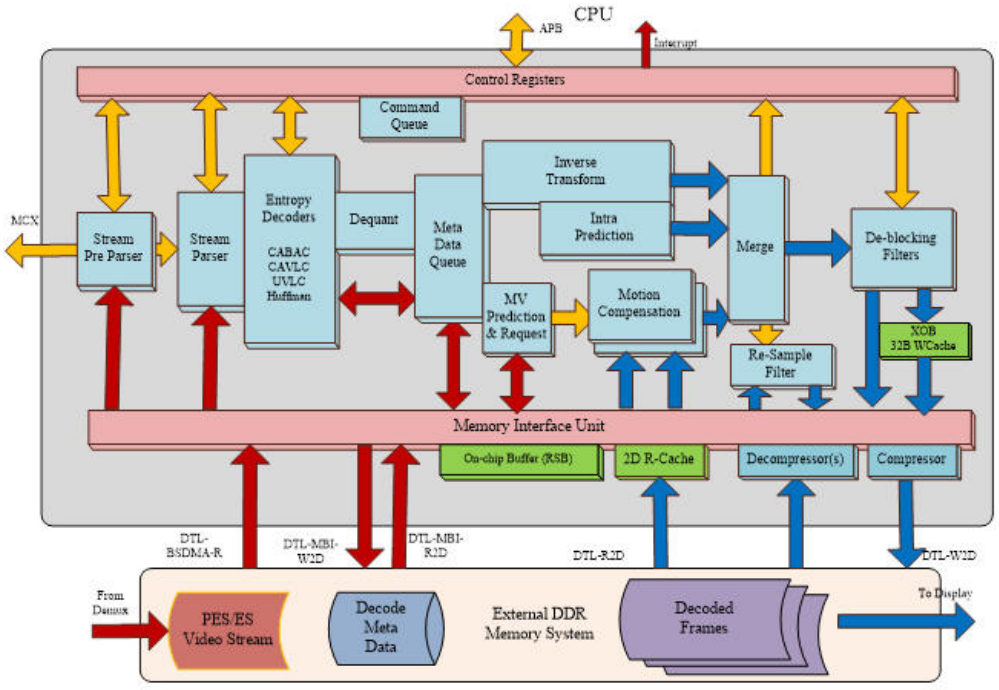
Features

- HEVC/H.265 MP@L5.1 (4KP60)
- PES or ES stream input
- High Latency Tolerance (CPU & Memory)
- Low CPU load
- Low Memory Bandwidth
- Robust Error Resilience controlled by Firmware
- Mature IP Silicon proven in multiple mass production STB and DTV SoCs down to 28nm
- Production Verified Firmware
- Extensively verified with a large library of third party test streams.



Operation

- CS8120 operates under direction of firmware
- Firmware pre-decodes headers and banks configuration commands
- Low CPU load allows CPU to run other hardware blocks in the system



CS8120 Block Diagram

Deliverables

- Bit accurate C models
- Verilog RTL and production firmware
- Synthesis scripts
- Self-checking test environment
- Datasheet and user manual

+44 28 95 609 600

info@amphionsemi.com

www.amphionsemi.com